REMARKS

Claims 22 and 28 are rejected under 35 USC §102(e) as being anticipated by Hebbalalu et al., U.S. 6,130,719.

Hebbalalu et al. '719 describes a method of recovering synchronization signals contained in a composite video signal. The synchronization signals are generally represented by voltage levels less than the blanking level of the video signal, and display data is represented by blanking level. A digital circuit controls a biasing circuit to generate a biasing voltage. A video signal is biased using the biasing voltage and the resulting biased video signal is provided as an input to an operational amplifier. A second input of the operational amplifier is driven by a reference voltage. The digital circuit monitors the output of the operational amplifier and controls the biasing voltage to cause the operational amplifier to clip the display data from the biased video signal and generate a signal representing synchronization signals.

In contrast, independent claims 22 and 28 recite determining whether the average value of one of said time-varying portions is substantially lower or the same as, but higher than the lower DC value detected within the time-equivalent of a last segment of video. Hebbalalu et al. '719 does not teach or suggest these essential features of the above mentioned claims.

The Examiner states that the clamping circuit 120 of the '719 patent determines a substantially time varying signal. However, the clamping circuit 120 recovers the synchronization signals and may include a biasing circuit 220, digital circuit 230, and operational amplifier 250. The digital circuit 230 can be used to examine the output and determine the necessary biasing voltage to clamp the input video signal to cause operational amplifier to

generate the synchronization signals. The digital circuit 230 includes boundary registers 610, pulse-type detection circuit 620, clamp state machine 650, and control circuit 630.

The pulse-type detection circuit 620 receives the output of operational amplifier 250 and determines whether a valid pulse is present. The pulse can be either HSYNC or VSYNC. The parameters in boundary registers 610 may be used to determine whether a received signal represents a HSYNC or VSYNC signal. The number of clocks between 2 falling edges of the composite signal may be counted and compared to upper and lower bounds. If the number of clocks falls within the bounds, a valid HSYNC pulse may be determined to exist. The duration of the HSYNC width may also be specified in the registers.

Similarly, a valid VSYNC may also be detected. VSYNC start is detected by counting the number of clocks the composite sync signal is determined to be at a low logic level. This is compared to a programmable minimum bound, and if the count exceeds this bound, VSYNC is determined to be present. The reception of VSYNC and HSYNC pulses may be communicated to clamp state machine 650. The presence of valid or invalid pulses may also be indicated to clamp state machine 650. A pulse may be invalid if the pulse duration represents neither a HSYNC pulse nor a VSYNC pulse.

There is also no discussion that the clamping circuit 120, and in particular the digital circuit 230 of the '719 patent, determining whether the average value of one of the time-varying portions is substantially lower or the same as, but higher than the lower DC value detected within the time-equivalent of a last segment of video.. As described, digital circuit 230 utilizes various clock edge analysis to make its determination. This is quite different from the invention, where slope analysis (differentiating the signal) is used to determine synchronization signals.

Determining a pulse is valid by using clock edges and using slope analysis to accomplish that task is quite different. Thus, Hebbalalu et al. '719 does not anticipate claims 22 and 28.

Claims 17-20, 23-25, and 27 are rejected 35 USC §103(a) as being unpatentable over Hebbalalu et al. '719 in view of Hulvey, US 5,844,622.

Hulvey '622 describes a digital video horizontal synchronization pulse detector and processor comprising pulse detector for generating a timing pulse in response to each horizontal synchronization pulse. A sync position error device generates a time position error signal for each timing pulse relative to a corresponding window pulse. A window pulse generator generates the window pulses and limits the time position error signals to a maximum value.

Claims 17, 19-20, 23-25, and 27 recite a time window for determining whether the output pulse is produced at a predetermined rate expected for the series of synchronization pulses and a voltage window for determining whether the average value of one of the time-varying portions is substantially lower or the same as, but higher than the lower DC value detected within the time-equivalent of a last segment of video.

As described above regarding Hebbalalu et al. '719, there is also no discussion that the clamping circuit 120, and in particular the digital circuit 230 of the '719 patent, determines whether the average value of one of said time-varying portions is substantially lower or the same as, but higher than the lower DC value detected within the time-equivalent of a last segment of video.. Moreover, whether the digital circuit 230 determines whether said output pulse is produced at a predetermined rate expected for the series of synchronization pulses

As described, digital circuit 230 utilizes various clock edge analysis to make its determination. This is quite different from the invention, where slope analysis (differentiating

the signal) is used to determine synchronization signals. Determining a pulse is valid by using clock edges and using slope analysis to accomplish that task is quite different. Thus, Hebbalalu et al. '719 does not anticipate claims 22 and 28.

Hulvey '622 describes a window generator circuit 54 that generates a window pulse 36 which is used to determine whether or not the local horizontal counter 48 is locked to the external horizontal sync pulse 30 and the relative timing or phase error of the external horizontal sync pulse 30 with respect to the window pulse 36. The window generator circuit 54 is configured to generate a window pulse 36 during which the external horizontal sync pulse 30 should occur and is preferably set to occur during counts 22 to 37 of the horizontal counter 48. The window generator circuit 54 also places limits on the maximum value for the phase or timing error.

However, the window generator of Hulvey '622 does not teach determining whether said output pulse is produced at a predetermined rate expected for the series of synchronization pulses. Moreover, there is no discussion in Hulvey '622 that the window generator determines whether the average value of one of said time-varying portions is substantially lower or the same as, but higher than the lower DC value detected within the time-equivalent of a last segment of video. Therefore, the combination of Hebbalalu et al. '719 and Hulvey '622 does not render obvious claims 17, 19-20, 23-25, and 27.

As to claim 18, it is dependent on claim 17. Therefore, claim 18 is also allowable for the same reasons argued with respect to claim 17.

Claims 26 are rejected under 35 USC §103(a) as being unpatentable over Hebbalalu et al. '719 in view of Hulvey '622 and further in view of Narusawa, US 4,792,852.

Narusawa '852 describes a vertical synchronizing signal detection circuit that detects a vertical synchronizing signal from a television signal by detecting the level of the television signal by sampling the television signal at a plurality of sample points established in a plurality of successive horizontal scanning periods. A pattern of level of the television signal during the successive horizontal scanning periods is compared with a reference pattern on the condition that synchronizing signals each discriminating a horizontal scanning period are accurately detected during these horizontal scanning periods. An erroneous detection of a false vertical synchronizing signal caused by noise or dropout can be prevented.

Claim 26 also recites determining whether the output pulses are produced at a predetermined rate expected for the series of synchronization pulses and determining whether the average value of one of the time-varying portions is substantially lower or the same as, but higher than the lower DC value detected within the time-equivalent of a segment of video. Narusawa '852 does not address these deficiencies of Hebbalalu et al '719 and Hulvey '622. Therefore, the proposed combination of Hebbalalu et al. '710, Hulvey '622, and Narusawa '852 does not render obvious claim 26.

In view of the above amendments and for all the reasons set forth above, the Examiner is respectfully requested to reconsider and withdraw the rejections made under 35 U.S.C. §102 and 103. Accordingly, an early indication of allowability is earnestly solicited.

If the Examiner has any questions regarding matters pending in this application, please feel free to contact the undersigned below.

Respectfully submitted,

Reg. No. 47,259

Matthew E. Connors
Registration No. 33,298
Gauthier & Connors LLP
225 Franklin Street, Suite 3300
Boston, Massachusetts 02110
Telephone: (617) 426-9180
Extension: 112